

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-13. (Canceled)

14. (Currently Amended) A semiconductor device comprising:

a wiring substrate having an upper surface, a plurality of first electrodes formed on the upper surface, a plurality of second electrodes formed on the upper surface, and a lower surface opposite the upper surface;

a memory chip having a first main surface, the first main surface having a substantially rectangular shape with two long sides having a greater length than two short sides, a respective plurality of first bonding terminals disposed on the first main surface along each of the two short sides, and a first back surface opposite the first main surface;

a microcomputer chip having a second main surface, the second main surface having a substantially square shape with four sides, a respective plurality of second bonding terminals disposed on the second main surface along each of the four sides, and a second back surface opposite the second main surface;

a respective plurality of first wires connecting each plurality of first bonding terminals with a corresponding group of the first electrodes, respectively; and

a respective plurality of second wires connecting each plurality of second bonding terminals with a corresponding group of the second electrodes, respectively;

wherein the second electrodes are arranged closer to an outer periphery of the wiring substrate than the first electrodes;

wherein the memory chip is mounted over the upper surface of the wiring substrate, inwardly from the first electrodes, with the first back surface facing the upper surface of the wiring substrate;

wherein the microcomputer chip is mounted over the first main surface of the memory chip with the second back surface facing the first main surface of the memory chip;

wherein the second bonding terminals include an external interface terminal electrically connected for electrical connection to outside of a system comprising the memory chip and the microcomputer chip the semiconductor device, and an internal interface terminal electrically connected with the memory chip;

wherein the total number of second bonding terminals is substantially greater than that of the first bonding terminals; and

wherein a length of each of the four sides of the microcomputer chip is greater than that of each of the two short sides of the memory chip and shorter than that of each of the two long sides of the memory chip, such that the mounted microcomputer chip covers a portion of each of the two long sides of the memory chip and covers no portion of the first bonding terminals of the memory chip.

15. (Previously Presented) The semiconductor device according to claim 14, wherein two opposing sides of the four sides of the microcomputer chip are adjacent to the two long sides of the memory chip, respectively, and the two opposing sides of the microcomputer chip extend substantially equally beyond the two long sides of the memory chip, respectively.

16. (Previously Presented) The semiconductor device according to claim 14, wherein the microcomputer chip, the memory chip, the upper surface of the wiring substrate, the first wires and the second wires are sealed with a mold resin.

17. (Previously Presented) The semiconductor device according to claim 14, wherein the memory chip has a function of an SRAM, a DRAM or a flash memory.

18. (Previously Presented) The semiconductor device according to claim 14, wherein the device includes a plurality of solder bumps connected to the lower surface of the wiring substrate, and wherein data, which is output through said external interface terminal of the microcomputer chip, is transmitted outside of the system through at least one solder bump.

19. (Previously Presented) The semiconductor device according to claim 14, wherein an additional semiconductor chip is mounted over the upper surface of the wiring substrate, and the memory chip is stacked over the additional semiconductor chip.

20. (Previously Presented) The semiconductor device according to claim 19, wherein an under-fill resin is filled in a gap between the additional semiconductor chip and the wiring substrate.